AMENDMENTS TO THE CLAIMS

Please cancel claim 5 without prejudice.

1. (CURRENTLY AMENDED) An apparatus for memory error control coding comprising:

a ~~first~~ syndrome encoder circuit configured to (i) receive a read data signal and a read parity signal and (ii) generate a first syndrome signal in response to ~~a~~ said read data signal and ~~a~~ said read parity signal;

a bypass circuit configured to (i) receive said first syndrome signal and a bypass signal and (ii) generate a second syndrome signal in response to said first syndrome signal and ~~a~~ said bypass signal, wherein said bypass circuit comprises one or more logic gates configured to (i) receive said first syndrome signal at a first input, (ii) receive said bypass signal at a second input and (iii) present said second syndrome signal at an output; ~~and~~

a ~~second~~ detector circuit configured to (i) receive said second syndrome signal, (ii) detect an error when bits of said second syndrome signal are not all the same state and (iii) generate one or more single error signals when a single bit error is detected in said read data and said read parity signals, a double error signal when an error is detected in two bits of said read data and read parity signals, and an error detected signal when either one of said one or more single error signals or said

double error signal are asserted in response to said second syndrome signal;

a locator circuit configured to (i) receive said second syndrome signal and (ii) generate an error location signal in response to said second syndrome signal, wherein said error location signal (i) is generated in response to fewer than all of said bits of said second syndrome signal and (ii) describes a location of a single bit error detected in said read data and said read parity signals; and

a corrector circuit configured to (i) receive said read data signal, said read parity signal, said error location signal and said one or more single error signals and (ii) generate a corrected representation of said read data and said read parity signals in response to said error location signal when a single bit error is detected.

2. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein all bits of said first syndrome signal are at a particular state when no error is detected in said read data and said read parity signals and said particular state comprises a digital 1.

3. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said apparatus is configured to present said read data and parity signals at an output when no error is detected in said read data and said read parity signals.

4. (CURRENTLY AMENDED) The apparatus according to claim 1, further comprising a memory circuit configured to (i) receive a data input signal and a parity input signal during a write operation and (ii) present said read data and said read parity signals during a read operation.

5. (CANCELED)

6. (CURRENTLY AMENDED) The apparatus according to claim 1, ~~further comprising a~~ said corrector circuit is further configured to ~~generate a~~ present said read data and said read parity signals as said corrected representation of said read data and said read parity signals ~~in response to said error location signal when a single bit~~ when no error is detected by said detector circuit.

7. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said ~~second~~ locator circuit and said detector circuit ~~is~~ are configured to invert each of said bits of said second syndrome signal.

8. (ORIGINAL) The apparatus according to claim 1, further comprising:

an encoder circuit configured to generate ~~said~~ a parity signal in response to a data input signal, wherein said encoder circuit comprises a type selected from the group consisting of (i)

non-inverting exclusive-OR gates, (ii) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (iii) inverting exclusive-OR gates, (iv) inverting exclusive-OR gates with an output inverted by a NOT gate, (v) non-inverting exclusive-NOR gates, (vi) inverting exclusive-NOR gates, (vii) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, and (viii) inverting exclusive-NOR gates with an output inverted by a NOT gate.

9. (CURRENTLY AMENDED) The apparatus according to claim ~~5~~1, wherein said ~~second~~ detector circuit comprises:

one or more OR gates configured to receive an inverse of said second syndrome signal and present said error detected signal;

one or more exclusive-OR gates configured to receive an inverse of said second syndrome signal and present an intermediate signal;

one or more AND gates configured to present said one or more single error ~~signal~~ signals in response to said error detected signal and said intermediate signal; and

an AND gate configured to present said double error signal in response to said error detected signal and an inverse of said intermediate signal.

10. (CURRENTLY AMENDED) The apparatus according to claim 9, wherein said one or more single error ~~signal comprises~~ signals comprise a multi-bit digital signal.

11. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said first syndrome signal is generated using a type of syndrome encoder selected from the group consisting of (i) non-inverting exclusive-OR gates, (ii) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (iii) inverting exclusive-OR gates, (iv) inverting exclusive-OR gates with an output inverted by a NOT gate, (v) non-inverting exclusive-NOR gates, (vi) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, (vii) inverting exclusive-NOR gates, and (viii) inverting exclusive-NOR gates with an output inverted by a NOT gate.

12. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said one or more logic gates of said bypass circuit are configured to (i) present each of said bits of said second syndrome signal having a state determined by a corresponding bit of said first syndrome signal in response to said bypass signal having a first state and (ii) present all of said bits of said second syndrome signal having the same state in response to said bypass signal having a second state.

13. (PREVIOUSLY PRESENTED) The apparatus according to claim 12, wherein said one or more logic gates are selected from the group consisting of AND, NAND, NOR, and OR gates.

14. (CURRENTLY AMENDED) An apparatus for memory error control coding comprising:

means for generating a first syndrome signal in response to a read data signal and a read parity signal;

means for generating a second syndrome signal in response to said first syndrome signal and a bypass signal, wherein (i) each bit of said second syndrome signal has a state determined by a corresponding bit of said first syndrome signal when said bypass signal is in a first state and (ii) all bits of said second syndrome signal have the same state when said bypass signal is in a second state; ~~and~~

means for (i) detecting an error when bits of said second syndrome signal are not all the same state and (ii) generating an error location signal, an error detected signal, a double error signal and one or more single error signals in response to said second syndrome signal, wherein said error location signal (i) is generated in response to fewer than all of said bits of said second syndrome signal and (ii) describes a location of a single bit error detected in said read data and said read parity signals; and

means for generating a corrected representation of said read data and said read parity signals in response to said error location signal when a single bit error is detected.

15. (CURRENTLY AMENDED) A method for memory error detection and correction comprising the steps of:

(A) generating a first syndrome signal in response to a read data signal and a read parity signal;

(B) generating a second syndrome signal in response to said first syndrome signal and a bypass signal, wherein (i) each bit of said second syndrome signal has a state determined by a corresponding bit of said first syndrome signal when said bypass signal is in a first state and (ii) all bits of said second syndrome signal have the same state when said bypass signal is in a second state;

(C) detecting an error when bits of said second syndrome signal are not all the same state; and

(D) generating an error location signal, an error detected signal, a double error signal and one or more single error signals in response to said second syndrome signal, wherein said error location signal (i) is generated in response to fewer than all of said bits of said second syndrome signal and (ii) describes a location of a single bit error detected in said read data and said read parity signals.

16. (CURRENTLY AMENDED) The method according to claim 15, wherein all of said bits of said second syndrome signal are at a particular state when no error is detected in said read data and said read parity signals and said particular state comprises a digital 1.

17. (PREVIOUSLY PRESENTED) The method according to claim 15, further comprising the step of:

bypassing said error location signal generating step in response to a predetermined state of said bypass signal.

18. (CURRENTLY AMENDED) The method according to claim 15, wherein step (C) further comprises the sub-steps of:

generating ~~a~~ said one or more single error ~~signal~~ signals when a single bit error is detected in said read data signal or said read parity signal;

generating ~~a~~ said double error signal when an error is detected in two bits of said read data ~~signal or~~ and said read parity ~~signal~~ signals; and

generating ~~an~~ said error detected signal when either one of said one or more single error ~~signal~~ signals or said double error signal are generated in response to said second syndrome signal.

19. (CURRENTLY AMENDED) The method according to claim 15, further comprising the step of:

presenting said read data and said read parity signals when no error is detected in said read data and parity signals.

20. (CURRENTLY AMENDED) The method according to claim 15, further comprising the step of:

generating a corrected representation of said read data and said read parity signals in response to said error location signal when said single bit error is detected.

21. (PREVIOUSLY PRESENTED) The apparatus according to claim 12, wherein said bypass circuit is configured to present all of said bits of said second syndrome signal as a digital 1 in response to said bypass signal having said second state.

22. (CURRENTLY AMENDED) An apparatus for memory error control coding comprising:

a syndrome encoder circuit configured to (i) receive a read data signal and a read parity signal and (ii) generate a syndrome signal in response to ~~a~~ said read data signal and ~~a~~ said read parity signal, wherein said syndrome encoder circuit comprises a type of syndrome encoder selected from the group consisting of (i) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (ii) inverting exclusive-OR gates, (iii) inverting exclusive-OR gates with an output inverted by a NOT gate, (iv) non-inverting exclusive-NOR gates, (v) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, (vi) inverting exclusive-NOR gates, and (vii) inverting exclusive-NOR gates with an output inverted by a NOT gate; and

a second circuit configured to (i) detect an error when bits of said syndrome signal are not all the same state and (ii) generate an error location signal in response to said syndrome

signal, wherein said error location signal (i) is generated in response to fewer than all of said bits of said syndrome signal and (ii) describes a location of a single bit error detected in said read data and said read parity signals.

23. (PREVIOUSLY PRESENTED) The apparatus according to claim 22, wherein said second circuit comprises:

one or more OR gates configured to receive a complement of said syndrome signal and present an error detected signal;

one or more exclusive-OR gates configured to receive a complement of said syndrome signal and present an intermediate signal;

one or more AND gates configured to present a single error signal in response to said error detected signal and said intermediate signal; and

an AND gate configured to present a double error signal in response to said error detected signal and an inverse of said intermediate signal.